

Basic Technology Research Laboratories Nippon Electric Co., Ltd.  
4-1-1 Miyazaki, Takatsu, Kawasaki, Kanagawa 213, Japan

### Abstract

A deep-recess channel structure has been applied to high power FETs in order to improve performances above to K-band. Internally matched devices have exhibited 2W power output with 16% power-added efficiency at 18 GHz, and 165 mW with 3 dB associated gain at 29.5 GHz.

### Introduction

GaAs power FETs have been improved for several years, and these FETs have already been used for microwave communication systems. However, there have been urgent requirements to develop higher efficiency and higher output power GaAs FETs for K and Ka-band applications.

In order to realize high efficiency power FETs, deeply recessed channel structure, such as that of the previously reported super low-noise GaAs FET<sup>1</sup>, has been applied to the high power FETs. The pattern layout has also been arranged to reduce parasitic capacitance and inductance, and to drive each cell with the in-phase RF signal.

Good DC characteristics, such as 1.2 V saturation voltage and 100 mS/mm transconductance, were observed on the developed FETs.

The internally matched device exhibited 2 W power output with 3 dB associated gain at 18 GHz. The 30 GHz band device exhibited 165 mW power output and 7 dB maximum linear gain.

### Device structure and fabrication

The deeply recessed channel structure, which has been applied to new power FETs, is effective to decrease source resistance. It is expected that reduction in source resistance will increase both power output and power gain.

The basic pattern layout for the developed MESFET was made the same as that of the commercially available NE869 series FETs. The pattern layout was, however, slightly

modified, considering the reduction in parasitic capacitance and inductance and the improvement in RF signal phase uniformities in each cell.

Appearance of the new FETs is shown in Fig. 1. The 750- $\mu$ m-wide gate FET consists of ten 75- $\mu$ m-wide gate fingers with 20  $\mu$ m spacing between them. The gate and drain bonding pads were made small to 50  $\mu$ m squares, in order to reduce parasitic capacitance. The chip length was made shorter than that of NE869 series FETs to reduce source inductance.

The 6-mm-wide gate FET consists of 8 unit cells, each one of them corresponds to the 750- $\mu$ m-wide gate FET. The gate busbars and drain pads were connected to each other and chip width was made as narrow as possible. These arrangements are effective to improve RF signal phase uniformities in each cell.

The device fabrication processes are almost the same as those of the super low-noise FET<sup>1</sup>. The active layer carrier concentration is  $1.5 \times 10^{17} \text{ cm}^{-3}$ . A 0.5- $\mu$ m-long and 0.6- $\mu$ m-thick Al gate was formed in the deeply recessed region by liftoff technique with a self-alignment method. Recessed length was 2.5  $\mu$ m and depth was 0.4  $\mu$ m. The 0.4  $\mu$ m recessed depth is necessary to decrease the source resistance as well as to keep the source-to-drain breakdown voltage high. The recessed length was defined after experimental optimization, considering power output and power gain.

The source and drain electrodes were those of the Ni/AuGe system. Source-drain electrode spacing was 4  $\mu$ m. Finally, the whole surface was passivated by  $\text{SiO}_2$ .

### DC characteristics

The developed MESFETs exhibited a high transconductance and a low saturation voltage (about 1.2 V) due to low source resistance. Figure 2 shows drain current versus drain-to-source voltage DC characteristics. The 100 mS/mm transconductance  $g_m$  and the 12-15 V gate-to-drain

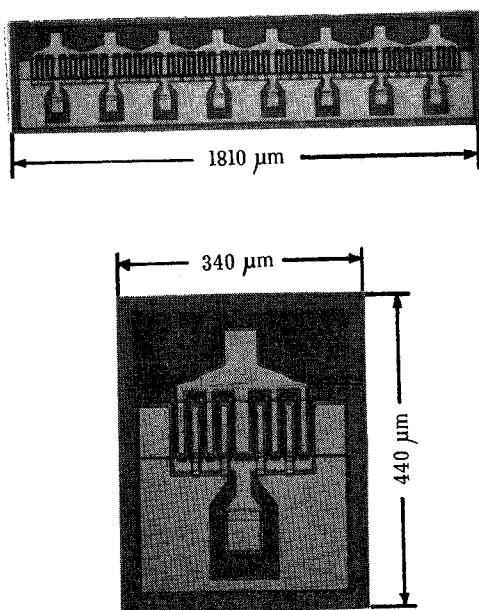


Fig.1 New FETs appearance (6-mm-wide gate FET (top) and 750- $\mu$ m-wide gate FET)

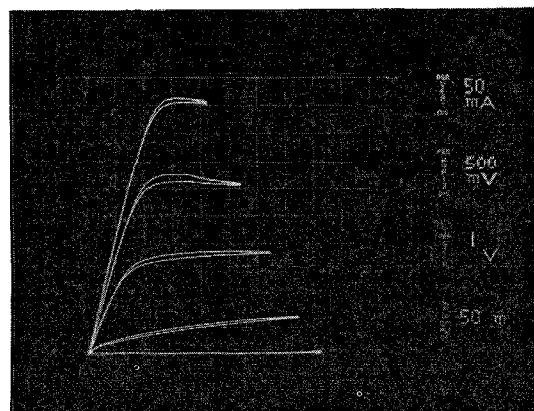


Fig.2 Drain current versus drain-to-source voltage DC characteristics. (gate width is 1.5 mm)

breakdown voltage  $BV_{GD}$  were observed on the developed FETs whose saturation current was about 300 mA/mm.

The drain-to-source breakdown voltage  $BV_{DS}$  was 30 V at pinchoff gate voltage and 17-18 V in the zero gate bias condition. These values are sufficiently high to ensure fail safe operation with more than 8 V drain voltage.

#### K-band internally matched FETs

The developed FETs were internally matched on chip carriers. An input matching network consists of series inductors and a parallel capacitor. An output matching network has a semidistributed form with open stubs. The capacitor is made of 0.1-mm-thick ceramic sheet with a 39 relative dielectric constant. All inductors are realized by gold bonding wires 30  $\mu$ m in diameter. The output open stubs, input terminal and output terminal are fabricated on 0.25-mm-thick alumina substrates.

Input/output power responses for internally matched devices in the K-band are shown in Fig. 3. The 3-mm-wide

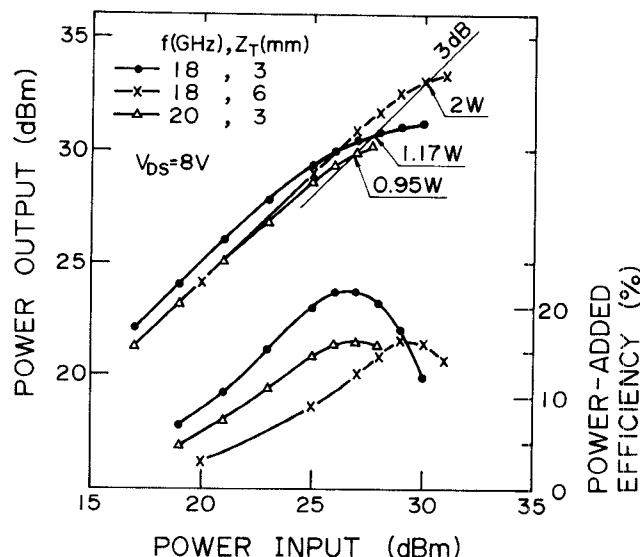


Fig.3 Input/output power responses for internally matched devices in the K-band.

gate device exhibited 1.17 W power output with 3 dB associated gain and 22 % maximum power added efficiency, and a 5 dB linear gain, at 18 GHz. This device was also demonstrated at 20 GHz after the trimming the input capacitor and the output open stubs to get 0.95 W power output with 3 dB associated gain and 16 % maximum power-added efficiency and a 4.2 dB linear gain. Furthermore, the 6-mm-wide gate device exhibited 2 W power output with 3 dB associated gain and 16 % maximum power-added efficiency with a 4.1 dB linear gain.

Figure 4 shows output power/frequency responses for these devices. The 3-mm-wide gate device covered the 17.6 to 19.1 GHz, and the 18.8 to 20.7 GHz frequency ranges with more than 0.6 W power output at 0.3 W input power level. The 6-mm-wide gate device covered the 17.4 to 18.6 GHz frequency range with more than 1.2 W power output at 0.6 W input power level.

The developed 3-mm-wide gate devices have a power output capability comparable to that of the 6-mm-wide gate NE869 series FETs<sup>2</sup>.

#### Ka-band internally matched FETs

A pair of microstrip-to-waveguide transformers were assembled in order to adapt the chip carrier devices to a Ka-band measurement system. Figure 5 shows the transformers and the chip carrier device.

A tapered ridge waveguide with one wave length at 30 GHz is used in the transformer. The ridge is isolated from the waveguide wall by thin dielectric film.

The performance for the pair of transformers was more than 18 dB return loss over the 28-33 GHz frequency range and 0.5 dB insertion loss, including a 50 ohm impedance 6-mm-long microstrip line.

A 750- $\mu$ m-wide gate FET is internally matched on a 4-mm-long chip carrier. Both input and output matching network are in microstrip form with open stubs, which are fabricated on 0.25-mm-thick alumina substrates.

Input/output power responses for the internally matched device in the Ka-band are shown in Fig. 6. There are two kinds of response obtained from different matching power levels. The 750- $\mu$ m-wide gate device exhibited 7 dB linear gain in a small signal matching case. This gain is sufficiently high to use in Ka-band applications. Under the power matching condition, the device exhibited 165 mW power output with 3 dB associated gain and 11.5 % maximum power-added efficiency, as well as 4.7 dB linear gain at 29.5 GHz.

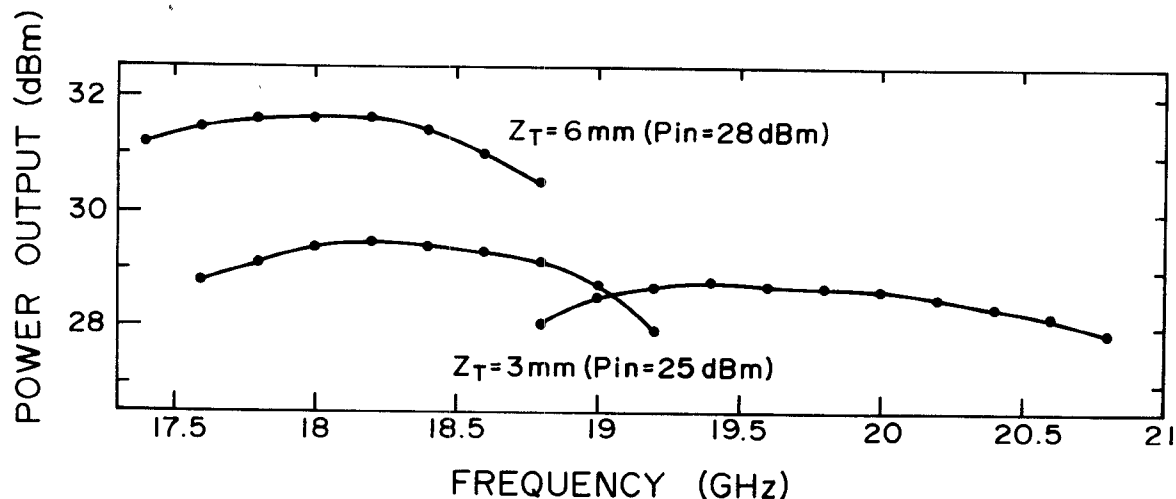


Fig.4 Output power/frequency responses for internally matched devices in the K-band.

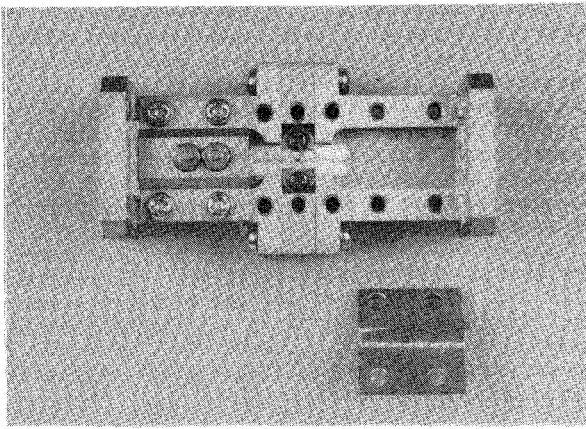


Fig.5 Ka-band transformers and chip carrier device.

Figure 7 shows output power/frequency response for this device in the large signal matching case. A more than 125 mW power output was obtained over the 29.2-30 GHz frequency range at 63 mW input power level.

The GaAs MESFETs, which had been demonstrated so far in the Ka-band, had a single gate finger usually adopted in low-noise FETs. The developed FETs, however, have interdigital gate fingers, so it is expected to achieve output power improvement by using the wide gate FET in the Ka-band.

#### Conclusion

A new power GaAs FET has been developed and demonstrated in the K and Ka-band. The application of the deeply recessed channel structure to power FETs resulted in low saturation voltage and high transconductance. The reduction of parasitic element value made it easy to design simple matching circuits also in the Ka-band.

In consequence, the internally matched developed FETs delivered 2 W power output at 18 GHz and 165 mW power output at 29.5 GHz. A sufficiently high linear gain (7 dB) was observed at 29.5 GHz.

These results indicate further capability of power FETs in the Ka-band, as well as in the K-band.

#### Acknowledgment

The authors wish to thank H. Takamizawa for supplying high dielectric constant substrates. They also wish to thank the staff personnel in the GaAs FET group for their valuable suggestions and discussions on the fabrication process and the microwave design. Thanks are also due to Dr. Y. Takayama, Dr. H. Katoh for their continuous support on this work and warm encouragement.

#### References

1. K. Ohata et al., "Super Low-Noise GaAs MESFETs with a Deep-Recess structure", IEEE Trans. Electron Device, Vol. ED-27, No.6, pp.1029-1034, June 1980.
2. J. Sone et al., "K-Band High-Power GaAs FET Amplifiers", IEEE Trans. Microwave Theory and Techniques, Vol. MTT-29, No. 4, pp.309-313, April 1981.

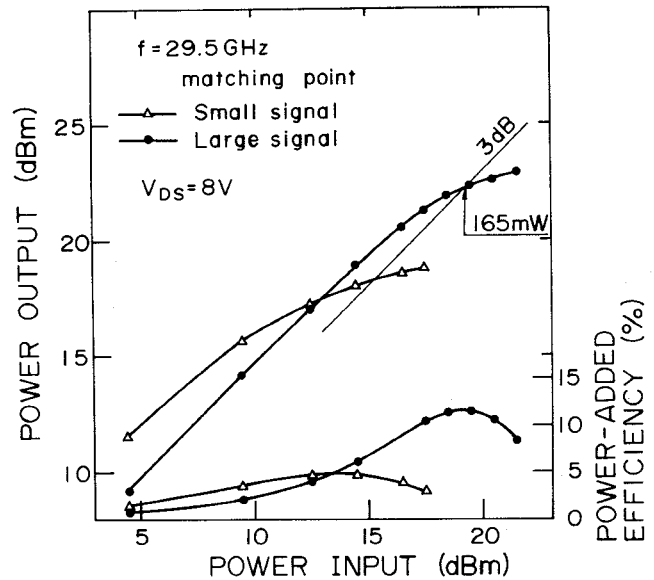


Fig.6 Input/output power responses for internally matched device in the Ka-band.

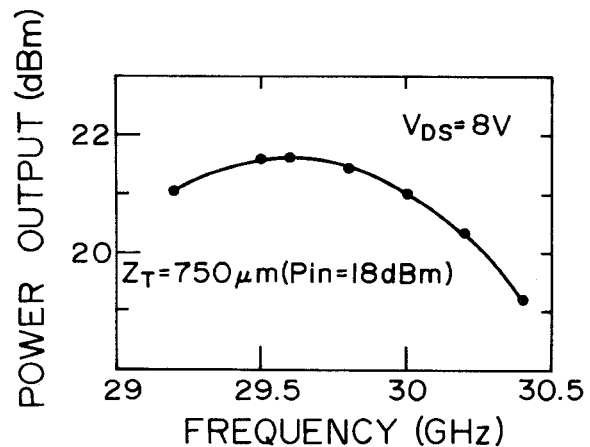


Fig.7 Output power/frequency responses for internally matched device in the Ka-band.